Listing of Claims

1. (Currently amended) A parallel processor comprising:

a plurality of non-volatile memory cells;

a plurality of processor elements, [at least one] each processor element being integrated with a non-volatile memory cell, [non-volatile memory cell corresponding with each of the processor elements, the] each processor elements [each] accessing data from a corresponding non-volatile memory cell that is most proximate to the processor element, [an at least one corresponding non-volatile memory cell,] and performing processing on the data.

2. (Original) The parallel processor of claim 1, wherein the non-volatile memory cells comprise magnetic memory cells.

3. (Original) The parallel processor of claim 1, wherein each processor element can access a plurality of non-volatile memory cells.

4. (Original) The parallel processor of claim 2, wherein each non-volatile memory cell is interfaced with a corresponding at least one dynamic random access memory (DRAM) cell.

5. (Currently amended) The parallel processor of claim 2, wherein each magnetic memory cell is formed adjacent to a substrate, and the corresponding processor element is formed in the substrate proximate and adjacent to the magnetic memory cell.

6. (Currently amended) The parallel processor of claim 4, wherein each magnetic memory cell is formed adjacent to a substrate, and the corresponding processor element and DRAM cell are formed in the substrate proximate and adjacent to the magnetic memory cell.

7. (Original) The parallel processor of claim 1, further comprising:
a master processor for receiving processed data from the plurality of processor elements.

8. (Original) The parallel processor of claim 7, wherein the master processor performs additional processing of the data.

9. (Original) The parallel processor of claim 1, further comprising:
an array of image sensors, an image sensor corresponding with each of the magnetic memory cells.

10. (Currently amended) The parallel processor of claim 9, wherein each image sensor receives image data that can be stored in [a] the corresponding non-volatile memory element.

11. (Original) The parallel processor of claim 10, wherein each processing element performs processing on the image data stored in a corresponding non-volatile memory element.

12. (Original) The parallel processor of claim 10, wherein the received image data is additionally stored in at least one DRAM cell corresponding with the non-volatile memory element.

13. (Original) The parallel processor of claim 9, wherein each image sensor is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element formed adjacent to the non-volatile memory element.

14. (Original) The parallel processor of claim 12, wherein each image sensor is formed adjacent to a corresponding non-volatile memory element, and each non-

volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element and DRAM cell formed adjacent to the non-volatile memory element.

15. (Currently amended) The parallel processor of claim 1, further comprising:

an array of display pixels, a display pixel corresponding with [at least one of the] a non-volatile memory cell[s].

16. (Currently amended) The parallel processor of claim 15, wherein each display pixel displays image data that is stored in [a] the corresponding non-volatile memory element.

17. (Currently amended) The parallel processor of claim 15, wherein each processing element performs processing on the image data stored in [a] the corresponding non-volatile memory element.

18. (Original) The parallel processor of claim 15, wherein the received image data is additionally stored in at least one DRAM cell corresponding with the non-volatile memory element.

19. (Original) The parallel processor of claim 15, wherein at least one display pixel receives image data from a plurality of non-volatile memory elements.

20. (Original) The parallel processor of claim 15, wherein each display pixel is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element formed adjacent to the non-volatile memory element.

21. (Original) The parallel processor of claim 18, wherein each display pixel is formed adjacent to a corresponding non-volatile memory element, and each non-

volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element and DRAM cell formed adjacent to the non-volatile memory element.

22. (Currently amended) A method of parallel processing, comprising:

storing data in a plurality of non-volatile memory cells;

processing the data with a plurality of processor elements which are integrated with the non-volatile memory cells, [at least one] each non-volatile memory cell corresponding with [each of the] a most proximate processor element[s], [the] each processor element[s each] accessing data from [an at least one] the corresponding non-volatile memory cell, and performing processing on the data.

23. (Currently amended) A computing system comprising:

a central processing unit;

a parallel processor connected to the central processing unit, the parallel processor comprising:

a plurality of processor elements, [at least one] each processor element being integrated with a non-volatile memory cell, [non-volatile memory cell corresponding with each of the processor elements, the] each processor elements [each] accessing data from the non-volatile memory cell that is most proximate to the processor element, [an at least one corresponding non-volatile memory cell,] and performing processing on the data.

24. (New) The parallel processor of claim 4, wherein a word line (WL) is connected to each non-volatile memory cell and a corresponding dynamic random access memory (DRAM) cell.

25. (New) The parallel processor of claim 24, the word line (WL) is connected a MRAM controlling transistor of the non-volatile memory and to a DRAM controlling transistor of the dynamic random access memory (DRAM) cell.

26. (New) The parallel processor of claim 5, wherein the corresponding processor element is formed in the substrate most proximate to the magnetic memory cell.

27. (New) The parallel processor of claim 6, wherein the corresponding processor element and DRAM cell are formed in the substrate most proximate to the magnetic memory cell.

28. (New) The parallel processor of claim 9, wherein the image sensor corresponding with a magnetic memory cell is the image sensor most proximate to the magnetic memory cell.

29. (New) The parallel processor of claim 15, wherein the display pixel corresponding with a non-volatile memory cell is the display pixel most proximate to the non-volatile memory cell.